REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this amendment, claims 1, 3, and 5-31, as amended, will remain in the application.

Specification

The specification has been amended to correct informalities.

Claim Objections

The claims have been amended to correct informalities.

Claim Rejections – 35 USC § 102

Claims 1-6, 19, 22, 23, and 25-29 were rejected under 35 U.S.C. 102(b) as being allegedly anticipated by Crouch et al. (U.S. Patent No. 5,995,731, hereinafter "Crouch").

Applicant teaches a tiered memory testing architecture including a first tier in which a single, centralized BIST controller is used to control memory tests on multiple memories by issuing generalized commands to sequencers at a second tier, each sequencer associated with memory modules sharing a common clock domain. At the third tier, memory interfaces, each associated with a corresponding memory module, handle specific interface requirements for each memory module, e.g., based on the specific timing requirements and physical characteristics of the memory modules. Advantages of this hierarchical BIST architecture is that area is conserved and overhead for the BIST controller only happens once, whether for testing a couple of memory modules or dozens.

Crouch describes a typical memory testing architecture in which a BIST controller is proved for each memory module. This approach is expensive in terms of area and overhead for the BIST controllers during testing. The Action cites col. 7, l. 56 to col. 8, l. 3 which describes a "combination parallel-sequential" operation. However, this refers to an architecture in which a BIST controller is provided for each memory module, and refers to staging BIST modules in a combination parallel-sequential manner.

Each of independent claim 1, 23, 25, and 27 recite a single BIST controller for issuing commands for testing multiple memory modules. Crouch does not describe such a system, but rather a typical BIST architecture in which a BIST controller is provided for each memory module. Accordingly, Applicant submits that these claims and their dependencies are allowable.

Claim Rejections – 35 USC § 103

Claims 7-18, 20, 21, 24, 30, and 31 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Crouch in view of Johnston et al. (U.S. Patent No. 6,272,588, hereinafter "Johnston").

Claims 7-18, 20, 21, 24, 30, and 31 depend respectively from one of allowable independent claims 1, 23, 25, and 27. Accordingly, Applicant submits that these claims are allowable with their base independent claims for the reasons stated above and for their additional limitations.

CONCLUSION

In light of the amendments contained herein, Applicants submit that the application is in condition for allowance, for which early action is requested.

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated 9/1/05

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